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Micro structured coupling elements for 3D silicon optical interposer

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ABSTRACT

Current trends in electronic industry, such as Internet of Things (IoT) and Cloud Computing call for high interconnect bandwidth, increased number of active devices and high IO count. Hence the integration of on silicon optical waveguides becomes an alternative approach to cope with the performance demands. The application and fabrication of horizontal (planar) and vertical (Through Silicon Vias - TSVs) optical waveguides are discussed here. Coupling elements are used to connect both waveguide structures. Two micro-structuring technologies for integration of coupling elements are investigated: µ-mirror fabrication by nanoimprint (i) and dicing technique (ii).
Nanoimprint technology creates highly precise horizontal waveguides with polymer (refractive index n_C = 1.56 at 650 nm) as core. The waveguide ends in reflecting facets aligned to the optical TSVs. To achieve Total Internal Reflection (TIR), SiO_2 (n_{Cl} = 1.46) is used as cladding. TSVs (diameter 20-40µm in 200-380µm interposer) are realized by BOSCH process[1], oxidation and SU-8 filling techniques. To carry out the imprint, first a silicon structure is etched using a special plasma etching process. A polymer stamp is then created from the silicon template. Using this polymer stamp, SU-8 is imprinted aligned to vertical TSVs over Si surface.Waveguide dicing is presented as a second technology to create coupling elements on polymer waveguides. The reflecting mirror is created by 45° V-shaped dicing blade.
The goal of this work is to develop coupling elements to aid 3D optical interconnect network on silicon interposer, to facilitate the realization of the emerging technologies for the upcoming years.

Keywords: Optical interposer, optical coupling elements, 3D optical interconnect network, micro structuring techniques, optical TSV, nanoimprint technology, 3D integration

1. INTRODUCTION

The continuous desire of users for faster electronics keeps on driving the advancement of the microelectronics industry. With the industry welcoming cloud computing, big data and IoT, etc. the need for faster data transmission is higher than ever before. As technology progressed, the device functionality kept increasing and hence the active device count has reached to millions. Microelectronic chips keep getting more dense and composite every time despite approaching the physical limits. With the increase in number of active devices, the amount of interconnects among the devices also tends to grow linearly. To keep the power requirement at lower end, a solution famously known as 'device scaling' was applied. Considering reduced chip area, the accommodation of even denser interconnect network is getting complex day by day. To cope with the interconnect area limitations, even the interconnect dimensions are being scaled down as the technology progresses. Recent ICs are equipped with multiple layers of metal. This solves the connectivity problem, however the denser interconnect network leads to signal integrity & interconnect delay issues[2]. An innovative approach is therefore required to cope with this challenge.

Already in 2002 ITRS roadmap[3] projected a huge increase in total wire length and decrease in transistor gate length over a couple of decades. These projections made it clear that the total interconnect wire length will be a limiting factor for the microelectronics industry growth. Learning from the real estate business model, the next logical step is to move the fabrication from 2D to 2.5D using an interposer chip. Ivo Bolsens et al. from Xilinx[4] were among the first ones to propose the lateral device distribution and ultimately a 3D (multi die stacked architectures) design[5]. Combination of these a.k.a. 5.5D (multiple 3D dies laterally connected with an interposer in 2.5D setup) is becoming more and more popular. In 2016, AMD® and Nvidia® came up with GPUs running with High Bandwidth Memory (HBM) using the concept of 5.5D

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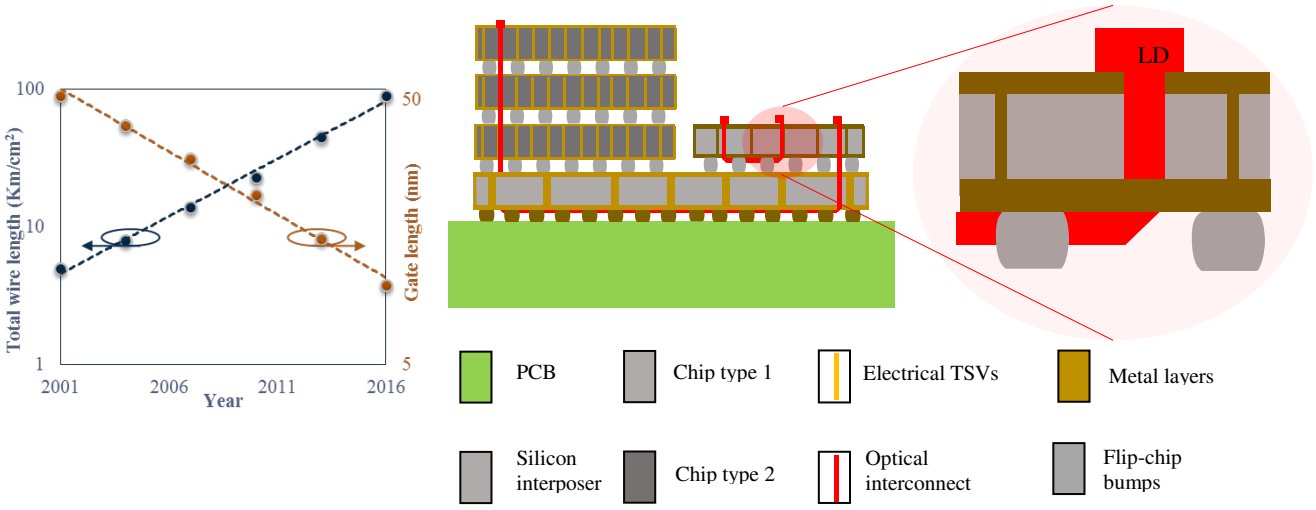
integration[6]. However there are several aspects facing physical and fabrication limits, and these needs to be addressed. 5.5D integrated circuits may provide a real solution because of better device scalability and improved packaging density. Development of high aspect ratio TSVs is one of the key aspects for interconnects in chip stacks[7]. Copper based electrical interconnects are traditional but a power hungry approach. A detailed interconnect power dissipation study of a microprocessor showed that interconnects use over 50% of the dynamic power in a chip[8].



(a) (b)

Figure 1 Transistor gate length and total wire length vs time in microprocessor (2002 ITRS) (a); Concept: 3D multi stacked integrated circuit as a solution and illustrative view of on silicon 3D optical interconnects (b)

Optical communication inherently provides the advantages which masks all the shortcomings of the electrical networks with a minor overhead (in terms of process change, opto-electrical and electro-optical conversions). E.g. the high interconnect density (& complexity) of the electrical network can be replaced with a simple optical network having significantly less interconnects, making it easier to design and simultaneously energy efficient. Having a huge bandwidth[9], a single optical interconnect could replace multiple electrical TSVs. To reduce the opto-electrical conversions, a couple of techniques are discussed in the following sections. However on a broader scale, moving to fully optical systems providing very high bandwidth and simpler interconnect architecture, i.e. chip to chip and chip to board communication is the next logical step. In addition to that, having a complete optical interconnect system will open the doors for a whole new set of applications, e.g. world's first electronic photonic processor by Berkely[10] is actually running at lighting fast speed! The advancement in transistors have extended the boundaries of modern day electronics until now. The upgrade to optical interconnects has the potential to revolutionize the IC development.

This paper describes the design and experimental investigation of micro structured planar optical interconnects and coupling elements, providing an end to end optical interconnect solution (supporting high bandwidth, larger number of devices and higher IO count) for cutting edge applications. Section 2 describes the main building block, i.e. optical interconnect design and fabrication. It is divided in three parts describing separate methods to fabricate optical TSVs and fabrication of coupling elements on each side of the horizontal interconnect using Nano Imprint Lithography (NIL) technique and dicing with V grooved blade. These processes are accompanied with their primary test results and towards the end the study is summarized.

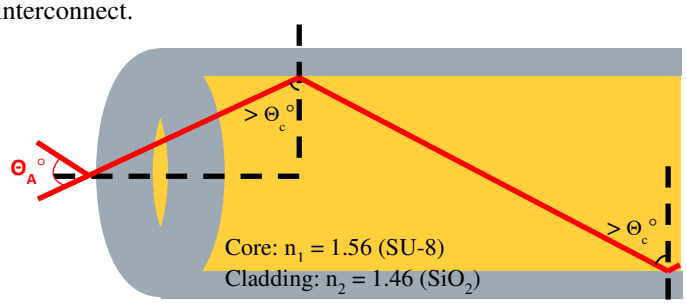
2. OPTICAL INTERCONNECT

An easier way to fabricate on chip optical components seems to be the missing piece of the jig-saw puzzle for high speed electronics. We have designed and developed an industry compatible fabrication process and extended the boundaries for fabrication possibilities of on chip optical components, making the fabrication easier for the next generation technology. Knowing the advantages of the optical interconnects, only one hurdle stood on the way to its arrival, i.e. convenience to fabricate. Cost efficient process to fabricate horizontal (planar waveguide) and vertical (TSV) interconnects and efficient coupling techniques to connect them between multiple planes was required to be developed. Design and layout rules needs to be upgraded for optimized optical layer applications. In order to exploit the advantages of the optical interconnects, robust coupling of optoelectronic converters (laser diodes and photo detectors) needs to be administered with utmost care.

Optical interconnect design can be classified in two main parts. 1) Vertical (optical TSV) and 2) horizontal interconnect. The concept regarding the optical interconnects remains the same for both, i.e. an on silicon object - capable of guiding the optical field within itself with low losses. For that it has to have a higher refractive index at core than surrounding (clad) region. Therefore a micro-structure forming an optical waveguide needs to be realized. To guide the light efficiently, the structure of the waveguide is inspired by an optical fiber. Both interconnect parts goes through design, etching and polymer filling steps. Optical TSV fabrication was developed and presented in our earlier research work[11]. The idea and process of optical TSV fabrication is briefly presented in section 2.1.

As far as vertical optical interconnect is concerned, there are total three possibilities for data transmission through an optical TSV. 1) Air filled TSV, i.e. free space transmission, where no filling is applied. Hence air (n_c=1 @ λ= 650 nm) becomes the core. The surrounding material is either Si or SiO_2, both of which have higher refractive indices. Therefore no TIR will be achieved. The reflection factor is determined by the difference of refractive indices and will always be smaller than 1. However, due to a very small size of the interconnect (of the order of several hundred microns), it provides acceptable data reception with very low Bit Error Rate (BER) (of the order of 10^{-6})[9]. 2) A combination of electrical and optical interconnects. Here the filling is again air. However, copper is deposited surrounding the air, providing twofold advantages. First, it can be used as a separate electrical conductor. At high frequencies, due to skin effect, the copper core is of no use anyways. And second, metals may have refractive index smaller than one, which helps guiding the light in the core medium. And 3) A dedicated optical waveguide with a polymer core (SU-8: n_c≈1.56 @ λ= 650 nm) surrounded with 2µm thick SiO_2 (n_{cl}≈1.46 @ λ= 650 nm) as cladding. Bulk silicon (n≈3.6 @ λ= 650 nm) has very high refractive index and to find a material which has higher refractive index than Si (in order to enable TIR) and with a possibility of filling, is very difficult. Hence in order to create an optical waveguide, Si has to be separated with a choice of fillable polymer material and a cladding material respective to its refractive index for the optical waveguide. SiO_2 was an adequate choice as cladding, since it can be either grown on Si (as thermal oxide) or deposited, and then the waveguide can be filled using the SU-8. This particular material selection provides a Δn ≈ 0.1, which is ample for an efficient light guiding interconnect. Of course, the higher the difference of refractive indices, the higher is the acceptance angle. However, higher acceptance angle and larger Δn corresponds to larger modal dispersion, limiting the bandwidth of the optical conductor. Hence it is a tradeoff between higher Δn (stronger guiding and lower loss due to bending and other environmental influences) and modal dispersion (less bandwidth). Forming only short connections in the millimeter range, a higher Δn is an intriguing choice.

However, only the third option of dedicated optical waveguide opens the doors to transfer the data in the third dimension and hence it is the main interest of this research work. In order to successfully apply the optical interconnect in a real 3D IC, it is mandatory to develop the ability to couple the light in third dimension. Selection of carefully crafted techniques provides efficient coupling for the optical interconnect in third dimension keeping the TIR intact throughout the interconnect.



$$n_1 \sin \Theta_1 = n_2 \sin \Theta_2 \quad \text{(i)}$$

Critical Angle:

$$\theta_c = sin^{-1} \frac{n_{SiO_2}}{n_{SU-8}} = sin^{-1} \frac{1.46}{1.56} = 69.37° \quad \text{(ii)}$$

Acceptance angle: $\Theta_A \approx 41.26°$

Figure 2 Total internal reflection boundaries using SU8 (core) and SiO_2 (clad)

2.1 Vertical optical interconnect (Optical TSV)

The design and fabrication of optical TSVs were carried out at our lab according to the process described in the work of S. Killge et al.[12] The technology concept is rather simple. The length and diameter of via were modeled for bandwidth, structure density and other efficiency related parameters. The structure sizes correspond to multimode waveguides. The acceptance angle can be calculated as shown in Figure 2 (≈41°), which is adequate for the high speed commercial Vertical Cavity Surface Emitting Laser diodes (VCSEL). In multimode waveguides, the mode dispersion prevails. This means that the propagation difference between fastest mode and slowest mode limits the data transmission capability. The transmission bandwidth depends on the difference of propagation time of these two modes. For our structures it can be calculated as following[9]:

$$t_{g,min} = \frac{L}{c_0} n_c \tag{iii}$$

Where $t_{g,min}$ is the propagation time for fastest mode, L is the length of waveguide (≈ 400 µm), c_0 is the velocity of light in vacuum and n_c is the refractive index of the core. $t_{g,max}$ is proportional to the n_{cl}. The propagation time difference between the extreme modes is ≈ 0.13 psec. This time difference results in pulse broadening. Now, considering the rectangular pulses (theoretically maximum wavelength containing waveform), the pulse broadening can be calculated by:

$$\sigma = \frac{t_{g,max} - t_{g,min}}{\sqrt{12}} \tag{iv}$$

Which leads to the baseband bandwidth:

$$f_B = \frac{0.2}{\sigma} \approx 4.94\, THz \tag{v}$$

This is theoretical bound for the 400 µm waveguides using the aforementioned materials. However, considering even a 1 mm long waveguide, the f_B still remains more than 1.8 THz. Hence, it is safe to consider that the data impairments due to mode dispersion in our designed structures will be considerably low.

After successful modeling, a corresponding layout is designed to incorporate the required vias on the mask. Then follows a photolithography step creating the basis for the anisotropic deep reactive ion etching (DRIE) (a.k.a. BOSCH) process, which etches through holes in the silicon wafer. A thermal oxidation process is then carried out to form the cladding layer. In order to keep the losses down, the modeling showed that the clad layer thickness should be at least half the thickness of the used wavelength[12]. To account for possible manufacturing tolerances, a safety factor was introduced for the cladding thickness and consequently approx. 2µm thick SiO_2 is grown over the edges of the TSVs. In order to fill the TSVs with SU-8, the back side of the wafer is covered with a temporary PDMS (Polydimethylsiloxane – a transparent polymer) membrane to facilitate the under vacuum filling. After curing the core of the waveguide (SU-8) with UV exposure, the backside membrane is stripped off and the wafer with the optical vertical interconnects is now ready to be coupled with its horizontal counterpart. The power loss measurements of the through silicon optical interconnects showed very promising results (2 – 3.5 dB power loss over ≈ 380µm long TSVs with 10:1 aspect ratio). The data transmission with <= 10^{-6} BER for 18 Gbps has already been demonstrated[9].

2.2 Horizontal optical waveguide and coupling elements

There are several techniques available to create horizontal interconnect, e.g. printing, proximity lithography, imprinting, etc[13]. However, in order to combine it with the vertical TSVs, a highly precise technique is required. The end of TSVs must meet at the ends of horizontal waveguides with guiding angles at the edges in order to redirect the light with minimum possible transmission losses.

The effect of bending: Since the coupling of optical waveguides involves two perpendicular data transmission directions, bending losses need to be studied. Considering the dimensions of these waveguides, a case of macro bending and its effects was analysed. At a bend, the propagation conditions change and parts of the optical signal are lost to the cladding and radiated. Considering the dimension, the waveguides with radius ≈ 20µm, behave as multimode fibers. The radius of curvature (R_C) is a decisive parameter to define the minimum possible curvature without significant losses for multimode fibers. For a given bend radius, higher NA results in smaller R_C because the light is guided more strongly in the core as

discussed before. The radius of curvature is the bend below which the losses increase rapidly. As shown in Figure 3(a), for a typical multimode fiber, the radius of curvature can be given as[14],

$$R_C = \frac{3{n_1}^2\,\lambda}{4\pi[{n_1}^2 - {n_2}^2]^{\frac{3}{2}}} \quad . \tag{vi}$$

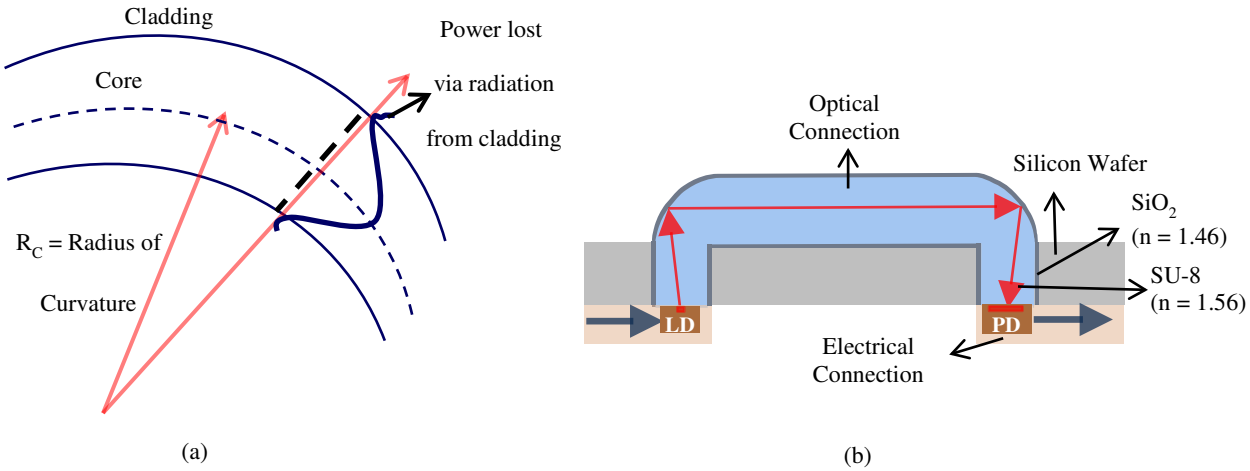


Figure 3 Mode field view at the bend showing the radius of curvature (a), and idea of 'U' shaped 3D interconnect with two bends

These bending losses can be reduced by intelligent selection of materials and wavelength(s). Using the known values: the refractive index for core SU-8 $n_1 = 1.56$, refractive index for cladding SiO_2 $n_2 = 1.46$ and wavelength of used light source $\lambda = 650$ nm; R_C appears to be $\approx 2.27\ \mu m$. The radius of curvature in our structures is more than ten times the calculated value of R_C, which assures that the bending losses due to the sharp turn is negligible. Primary measurement results show that most of the power loss occurs at the edges of the interconnects due to the mismatch of the transmitter and receiver placement and variation in primary beam placement at the entrance and beam collection at the receiver end.

Results from the theoretical calculations approve the construction scheme as shown in Figure 3(b). To create such a structure, two methods were used, i.e. 1.) Nano Imprint Lithography - NIL, and 2.) Dicing. Both methods have their advantages and disadvantages. While the NIL enables wafer level processing and supports really small structure sizes (of the order of several nano meters), it is a sophisticated method involving silicon master fabrication, multiple stamp fabrications and requires a specific apparatus to align and couple the structures with temperature and pressure. On the other hand, creating 45º angled reflecting elements (µ-mirror) using V shaped dicing blade requires precise alignment. In addition to that it is damaging the surface of the substrate. Therefore it is not compatible with the wafer level batch fabrication. However, using this method, one can calibrate the horizontal waveguide structures with fewer steps.

The important condition of the 3D optical interconnect is to have a reflecting element joining two perpendicular waveguides. It was met with both of these methods. Hence they have been examined for their efficiency and applicability. A third method is known as Moving Mask, where the mask and the substrate with photoresist are moved respectively to each other in a micron scale. This movement cross links the photoresist in a positive slope, creating a reflecting mirror element. This method is currently under research.

(a) Nano imprint technique

This technique permits low loss coupling elements for three dimensional signal transmission without any interruption. While the challenge in TSV fabrication was to achieve a straight sidewall profile of ≈ 90º, it changes for the horizontal waveguide fabrication. The sole purpose of this structure is to couple the light coming from the vertical interconnect. In order to keep most of the optical signal within the core material, a constant curved design was chosen (idea shown in Figure 3(b)). The constantly varying angle at both edges of the horizontal interconnect assists the light to reflect and keeps the propagation within the waveguide core region. To create the tunable slope, a process developed by K. Richter et al. [15,16] was used. It is formally known as Positive Profile Etching (PPE) process. The process can be classified as a sequence:

1) IE - Isotropic Etching (equal increase in etch depth and width), 2) AIE - Anisotropic Etching (only etch depth increase, hence positive angle is formed) and 3) cleaning step (stripping the polymer residues) using O_2 plasma. The exact process recipe can be found in the publication[16].

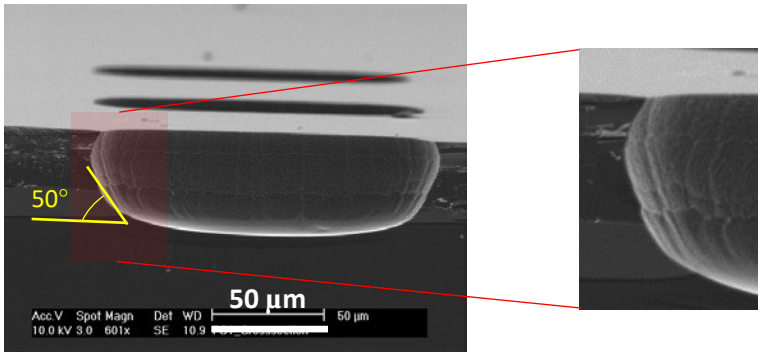


Figure 4 PPE Primary etch process result (left); magnified picture of structure edge and silicon beak (right)

The basic PPE process is tuned to generate a structure with a sidewall angle of 45°-50° as shown in Figure 4. The structures possess a tiny Si beak on top edges. In addition to that, the structures have minor scallops on the sidewalls and a moderate amount of surface roughness throughout the structure. This abnormalities of the etch structures may cause problems in forming the stamps required for the following imprint step. In order to remove these abnormalities and adjust the structure widths according to the design requirement, an additional post etching process step was developed. It comprises of a short anisotropic etch step, a cleaning step and at the end a considerably long (4 min) isotropic etch step. The process recipe can be found in Table 1. This overetch process rounds up the angles at the edge and provides smooth reflecting mirror surfaces, which are required to guide the light more efficiently.

Table 1 Overetch process (correction for PPE)

Step	Process parameters					
	Gas flow [SCCM]		Pressure [mT]	Coil/Platen Power [W]	Time [mm:ss]	Cycle (m:ss)
(1)AIE	C_4F_8	60	12	700/15	00:03	8x (1:04)
	$SF_6 + C_4F_8$	130 + 35	24	600/18	00:05	
(2) Cleaning	O_2	70	10	600/-	00:30	1x (0:30)
(3) IE	SF_6	130	28	600/9	04:00	1x (4:00)

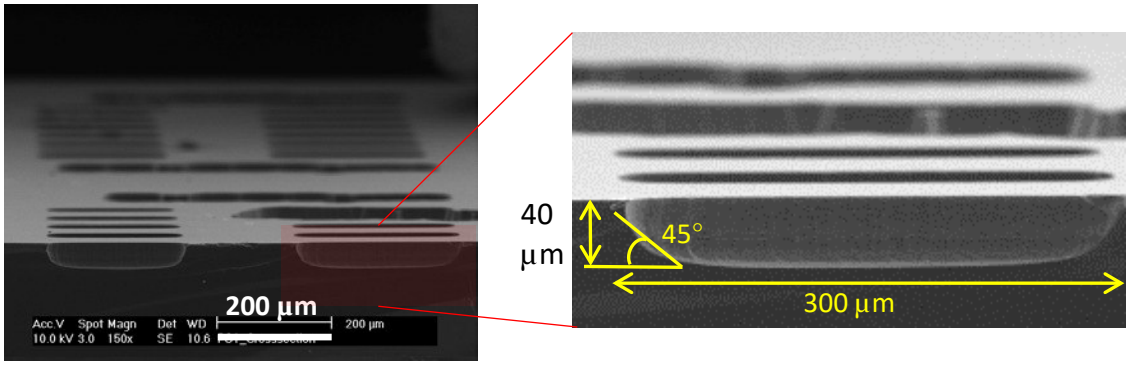


Figure 5 Etch result after post processing (smooth surface and silicon beak removed)

As shown in the Figure 5, the required shape is now achieved on silicon substrate, which resembles the shape of coupling element from Figure 3(b). Now, to transfer the pattern in SU-8, intermediate stamps are required. PDMS (Sylgard 184 silicon elastomer from Dow corning® - 10:1 mixture of silicon elastomer and curing agent) was chosen as polymer material for the intermediate stamps, because of its transparency in the UV spectrum and the flexibility after solidification. The last step in Nano Imprint Lithography - NIL, i.e., cross linking the SU-8 layer, requires UV exposure. Moreover, in order to achieve very small residue layer in NIL, a flexible material is preferred to squeeze out the excess SU-8.

Since the adhesion between Si and PDMS is very strong, a very thin polymer layer (of the order of 100-200 nm) is first deposited on Si using plasma polymerization process of C_4F_8 gas. Then the surface is covered with a thick PDMS layer followed by a curing step at 110ºC for 30 mins. A thin C_4F_8 layer greatly helps in the repealing process for stamp fabrication. Since the first stamp has the inverted patterns, a similar process is carried out to form a second stamp from the first (again a thin C_4F_8 layer followed by PDMS deposition and curing).

In order to achieve low transmission losses, the residue layer of SU-8 should be as small as possible. To reach to nm(s) thin residue layer, several techniques were utilized: (1) the substrate is first spin coated with SU-8 (resist thickness ≈ 30 µm). Successful pattern transfer was achieved using EVG 6200 series NIL tool. However, due to limited pressure (1000 mBar) and absence of heating options, the residue layer thickness was in several tens of microns range. Hence, another techniques which enabled higher pressure and temperature were carried out. (2) After spin coating, a soft bake of SU-8 at 70°C was performed which hardens the resist. It is specifically important to have a resist in solid phase, in order to achieve reproducibility. Here, the PDMS stamp is kept on the desired SU-8 surface and then pressure and temperature is applied gradually. For temperatures higher than 70°C, the un-crosslinked SU-8 becomes viscous again and because of the flexible nature of the PDMS stamp, the negative patterns are formed in SU-8. Excess material is squeezed away from the undesired regions because of high pressure. Then a UV exposure cures the SU-8 to form horizontal waveguides. This method can be combined with vertical TSV fabrication to generate the continuous 3D interconnects. As shown in the Figure 6, multiple lengths of horizontal waveguides were fabricated with a very small residue layer (of the order of several tens of nm). The downside of this method is that, due to mechanical alignment option, it is currently difficult to align the TSVs with other coupling elements. Hence, 3.) a flip chip bonder tool was used to carry out NIL. The tool enables pressure up to 60N/cm^2 surface area and can easily heat up to several hundred degree C. The downside here is the limitation of smaller sample size, because the tool is actually designed to bond dies. To summarize, the results of technique 2 and 3 were fairly similar. The tradeoff here was between the ability to align structures vs. the sample size.

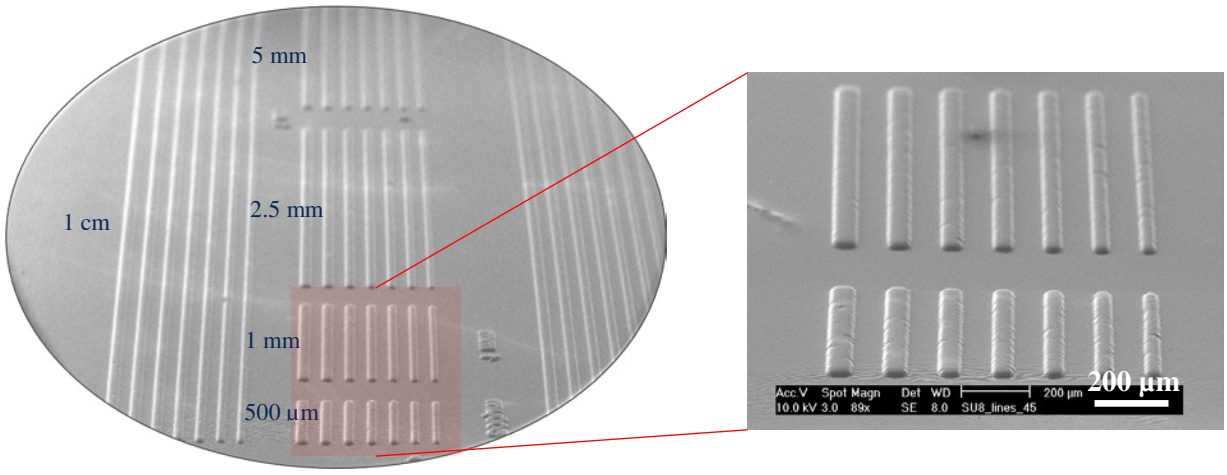


Figure 6 Horizontal SU-8 waveguides with coupling elements using nano imprint (a), and magnified SEM picture showing 500 µm and 1 mm waveguides (b)

(b) Dicing technique

Manufacturing of coupling elements on polymer waveguides using a V groove dicing blade is a subtractive method. First a generic horizontal waveguide overlapping the coupling regions is developed. This could be achieved by a simple spin on

of polymer and a proximity lithography step. Then as shown in the Figure 7, the dicing blade is aligned to the substrate at the intersection point of the horizontal and vertical interconnects and an incision is performed.

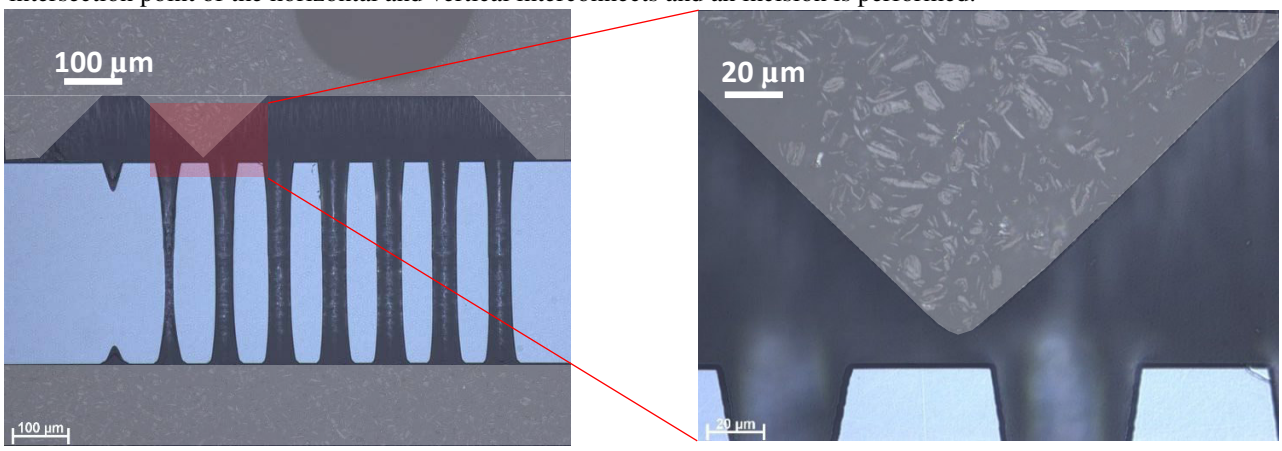


Figure 7 A complete 3D optical interconnect with dicing technique (left); the magnified view of the coupling element (right)

Because this technique relies on individual alignment for each interconnect, the process is time consuming and prone to several microns alignment errors. One another weakness of this method is that the dicing of the coupling element can only be in one direction at a time, while the imprinting technique can create multiple coupling elements in various directions over a larger surface area in one process step. However, the end profile of the structure via dicing through a V groove blade is rather supporting the concept of Total Internal Reflection (TIR). Hence this method is being worked on in parallel.

2.3 Characterization of the horizontal waveguides

As mentioned in section 2.1, the vertical TSVs were characterized for their optical transmission performance. Similarly a measurement setup was built to estimate the power loss between multiple lengths of the horizontal interconnects as shown in Figure 6. The waveguides were diced on the edges, revealing 500 µm, 1 mm, 2.5 mm and 5 mm lengths. A laser source of 660 nm VCSEL was used as input. Two multimode fibers (Ø 50µm core / Ø 125 µm cladding) were used to connect the waveguides with laser source and photo detector as shown in Figure 8. The result of attenuation measurement for various lengths of the horizontal waveguides is shown in Figure 9.

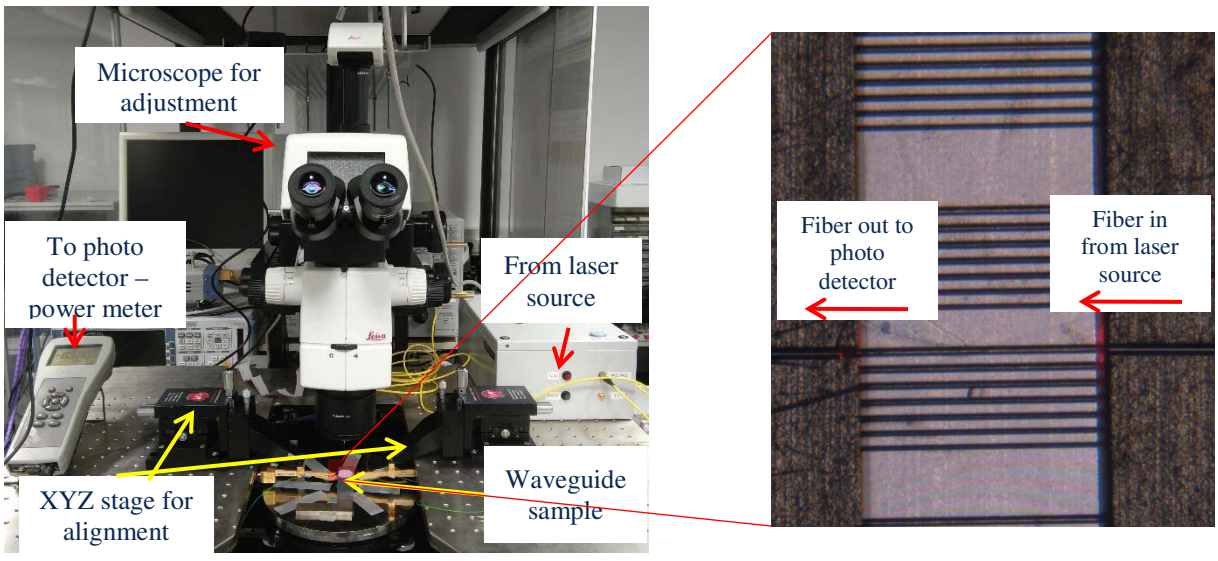


Figure 8 Laboratory setup for horizontal waveguide measurement (left) and 2.5 mm long waveguides under test (right)

The primary measurement revealed that the waveguides fabricated using imprint technology were capable of guiding light efficiently. Elementary estimate of the power loss was between 2.5-3.5 dB for every 500 µm waveguide length. This is comparable with the optical TSV measurements carried out earlier (mentioned in section 2.1).

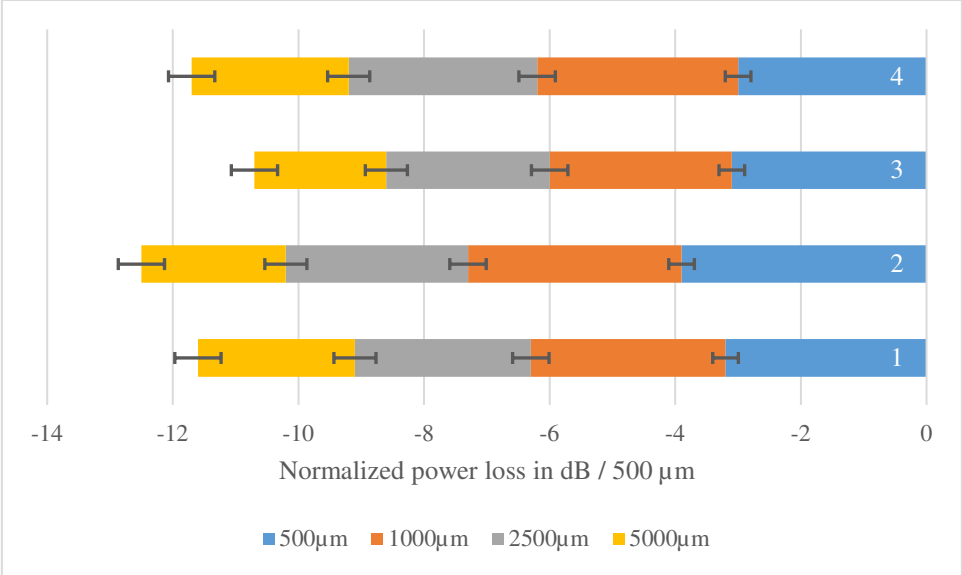


Figure 9 Horizontal waveguide attenuation: measurement results

There are various uncertainties and coupling losses present in the primary measurements, however it is seen from the results that the waveguide performance in vertical as well as horizontal direction is fairly similar. Nevertheless a more detailed investigation on the performance and data transmission capability are subject for further investigation.

3. CONCLUSION

Optical interconnects have the potential to provide huge bandwidths and increasing demand for faster microelectronics might just require this special attribute of the optical interconnects. The bandwidth of these interconnects is expected to be extremely high (theoretically as well as in practice - in hundreds of GHz). This paper presents several solutions to fabricate optical interconnects on silicon substrate. Development aspects of both types of interconnects (vertical TSV and horizontal waveguides) are presented here, along with their individual performance results. Overlooking the IO coupling losses, the light guiding behavior of the waveguides showed acceptable attenuation behavior (2-3.5 for every 500µm waveguide length). In addition, this paper provides several novel techniques to combine one directional interconnects with dedicated micro structured coupling elements to form an end to end 3D optical interconnect: nano imprinting and dicing. The main advantage of the nano imprinting technology is that it is easily adaptable to the waveguide lengths. According to various interconnect length requirements, a calculated change of layout design results in the exact horizontal dimension required to couple multiple vertical TSVs. This allows us to connect multiple 3D paths (e.g., daisy chain elements connecting multiple planes) on the chip without breaking the optical transmission. A complete 3D interconnect measurement is under further investigation. However the preliminary characterization was carried out in two steps. The optical TSV and horizontal waveguide measurements were performed separately. These measurements show that the horizontal waveguides are at par with the vertical TSV measurements, demonstrating that both independent components of the 3D interconnect system perform satisfactorily.

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